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| 10/574,829 | 04/06/2006 | Shunpei Yamazaki | 740756-2950 | 3691 |

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NIXON PEABODY, LLP
401 9TH STREET, NW
SUITE 900
WASHINGTON, DC 20004-2128

| EXAMINER | |
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| RAO, SHRINIVAS H | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/574,829 | YAMAZAKI ET AL. | |
| | Examiner | Art Unit | |
| | STEVEN H. RAO | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 March 2007*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/06/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

Acknowledgment is made of papers filed claiming priority from PCT/Jp-2004-016153 filed on October 25, 2004.

### *Information Disclosure Statement*

The Ids filed on April 06, 2006 has been considered and the initialed PTo-1449 made of record in the E-Red folder.

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 to 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yudasaka et al. ( U.S. Patent Publication No. 202/0179906, herein after Yudasaka, also cited by Applicants' in their IDS) in view of Bojkov et al. (U.S. Patent No. 5,947,783 herein after Bojkov)

1. With respect to claim1 Yudasaka describes a liquid crystal display device comprising:

a pair of substrates ( Yudasaka para 0003) ; a liquid crystal interposed between the pair of substrates; ( Yudasaka para 0003)a thin film transistor over one of the pair of substrates; ( Yudasaka para 0003 and a pixel electrode connected to the thin film transistor, wherein the thin film transistor comprises ( fig. 17):

Yudasaka mentions a gate electrode but does not specifically mention it (gate) of nanoparticles.

However Bojkov a patent from the same filed of endeavor, describes in its abstract ( col.5 lines 30-35) a gate electrode formed over the substrate by fusing conductive nanoparticles to provide films that have desired pixel structures, that can be used in display structures.

Therefore it would have been obvious to one of ordinary skill in the at the time of the invention to include Bojkov's a gate electrode formed over the substrate by fusing conductive nanoparticles in Yudasak's device. The motivation for the above inclusion is to provide films that have desired pixel structures , that can be used in display structures. ( Bojkov col.1 lines 43-47).

.

The remaining limitations of Claim 1 are :

a layer including at least one of silicon nitride and silicon oxynitride formed on

and in direct contact with the gate electrode, ( Bjvkov fig. 6,22) a gate insulating layer at least containing a layer comprising silicon oxide over the layer, (Bojkov col. 3 lines 14-15)and a semiconductor layer over the gate insulating layer. ( Bojkov fig.6 # 600).

With respect to claim 2 Yudasaka describes a liquid crystal display device comprising:
a pair of substrates, a liquid crystal interposed between the pair of substrates;
a thin film transistor over one of the pair of substrates; and a pixel electrode connected to the thin film transistor, wherein the thin film transistor comprises:
a gate electrode formed over the substrate by fusing conductive nanoparticles,

a first layer including at least one of silicon nitride and silicon oxynitride formed on and in direct contact with the gate electrode, a gate insulating layer at least containing a silicon oxide layer over the first layer, and

a semiconductor layer over the gate insulating layer;
(rejected for reasons under claim1 above) a wiring connected to at least one of a source and a drain; ( Yudasaka para 0188, fig.4) and a second layer including at least one of silicon nitride and silicon oxynitride formed to be on and in direct contact with the wiring ( Bjvkov col.3 lines 14—15), wherein the wiring formed by fusing conductive nanoparticles. ( Bojkov col. 5 lines 30-35).

With respect to claim 3 Yudasaka describes a liquid crystal display device comprising:
a pair of substrates; a liquid crystal interposed between the pair of substrates;
a first thin film transistor over one of the pair of substrates; a pixel electrode

connected to the thin film transistor; a driver circuit constructed by a second thin film transistor which comprises the same layer structure of the first thin film transistor; and a wiring extending from the driver circuit and connected to a gate electrode of the first thin film transistor, wherein the first thin film transistor comprises: the gate electrode formed over the substrate by fusing conductive nanoparticles, (rejected for reasons under claim1 above)a layer including at least one of silicon nitride and silicon oxynitride formed on and in direct contact with the gate electrode, a gate insulating layer at least containing a layer comprising silicon oxide over the layer, and a semiconductor layer over the gate insulating layer. ( rejected for reasons under claims1 -2 above).

With respect to claim 4 Yudasaka describes a liquid crystal display device comprising:
a pair of substrates; a liquid crystal interposed between the pair of substrates; a first thin film transistor over one of the pair of substrates; a pixel electrode connected to the thin film transistor; a driver circuit constructed by a second thin film transistor which comprises the a first layer including at least one of silicon nitride and silicon oxynitride formed on and in direct contact with the gate electrode, a gate insulating layer at least containing a silicon oxide layer over the first layer, and a semiconductor layer over the gate insulating layer; a wiring connected to at least one of a source and a drain; and a second layer including at least one of silicon nitride and silicon oxynitride formed on and in direct contact with the wiring, wherein the wiring formed by fusing conductive nanoparticles. ( rejected for reasons under claim 1-3 above).

With respect to claim 5 Yudasaka describes the liquid crystal display device according to any one of claims 1 to 4, wherein the conductive nanoparticles comprise Ag. ( well known in the art).

With respect to claim 6 Yudasaka describes the liquid crystal display device according to claim 2 or 4, wherein the semiconductor layer comprises at least one of hydrogen and halogen; and wherein the semiconductor layer is a semi-amorphous semiconductor having a crystal structure. ( Yudasaka para 00135).

With respect to claim 7 Yudasaka describes the liquid crystal display device according to claim 2 or 4, wherein the driver circuit comprises only an n-channel type thin film transistor. ( Bojkov col. 4 lines 46-47,fig. 10, # 1007).

With respect to claim 8 Yudasaka describes the liquid crystal display device according to claim 1 or 2, wherein the thin film transistor comprises the semiconductor layer including hydrogen and halogen and which is a semiconductor having a crystal structure, wherein the thin film transistor is capable of being operated in electric field effect mobility of from 1 cm2/V-sec to 15 cm2/V-sec.

With respect to claim 9 Yudasaka describes liquid crystal display device according to claim 3 or 4, wherein the first thin film transistor and the second thin film transistor comprise the semiconductor layer including hydrogen and halogen and which is a semiconductor having a crystal structure, wherein the first thin film transistor and the second thin film transistor are capable of being operated in electric field effect mobility of from 1 cm2/V-sec to 15 5 cm2/V-sec. ( Bojkov col.3 lines 64-67, Yudasaka para 00197).

With respect to claim 10 Yudasaka describes a liquid crystal television receiver comprising the liquid crystal display device according to any one of claims 1 to 4. (rejected for reasons under claims 1 to 4).

With respect to claim 11 Yudasaka describes a method for manufacturing a liquid crystal display device comprising the steps of: forming a gate electrode over a substrate having an insulating surface with a droplet discharge method; laminating a gate insulating layer, a semiconductor layer, and an insulating layer over the gate electrode; ( rejected for reasons under claims 1 to 4 above) forming a first mask in a position overlapping with the gate electrode with a droplet discharge method; forming a channel protective layer by etching the insulating layer by using the first mask; (Yudasaka para 0183) forming a semiconductor layer containing one conductivity type impurity;( Yudasaka figs.) forming a second mask in a region including the gate electrode with a droplet discharge method; etching the semiconductor layer containing one conductivity type impurity and the semiconductor layer; (Yudasaka para 00186) forming source and drain wirings with a droplet discharge method;( Yudasaka fig.11 33s and 33d) and etching the semiconductor layer containing one conductivity type impurity over the channel protective layer by using the source and drain wirings as masks. ( Yudasaka para 0187)

With respect to claim 12 Yudasaka describes a method for manufacturing a liquid crystal display device comprising the 30 steps of: forming a gate electrode and a connection wiring over a substrate having an insulating surface with a droplet discharge method; laminating a gate insulating layer, a semiconductor layer, and an insulating layer over the gate electrode; forming a first mask in a position overlapping with the gate electrode with a droplet discharge method; forming a channel protective layer by etching the insulating layer by using the first mask; forming a semiconductor layer containing one conductivity type impurity; forming a second mask in a region including the gate electrode with a droplet discharge method; etching the semiconductor layer containing one conductivity type impurity and the semiconductor layer; partially exposing the connection wiring by selectively etching the gate insulating layer; forming a source wiring and a drain wiring and connecting at least one of the source wiring and the drain wiring to the connection wiring at the same time; and etching the semiconductor layer containing one conductivity type impurity over the channel protective layer by using the source and drain wirings as masks. (rejected for reasons under claims

1-4 and `12).

With respect to claim 13 Yudasaka describes the method for manufacturing a liquid crystal display device according to claim 11 or 12, wherein the step of laminating a gate insulating layer, a semiconductor layer, and an insulating layer over the gate electrode is carried out without exposing to the atmosphere. (para 0039 e.g. CVD carried out in enclosed chamber).

With respect to claim 14 Yudasaka describes the method for manufacturing a liquid crystal display device according to claim 11 or 12, wherein the gate insulating film is sequentially laminated by a first silicon nitride film, a silicon oxide film, and a second silicon nitride film. ( Bojkov col.3 lines 14—15).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN H. RAO whose telephone number is (571)272-1718. The examiner can normally be reached on 8.30-5.30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Steven H Rao/
Examiner, Art Unit 2814

/Howard Weiss/
Primary Examiner, Art Unit 2814